CLAIMS:

Cancel the claims of record (1-12) and substitute new claims 21-40 as follows:

21. An integrated circuit (IC) supporting electrically programmable three-dimensional memory (EP-3DM)-based self-test (EP-3DMST), comprising:

a substrate circuit, said substrate circuit further comprising a circuit-under-test (CUT) and a peripheral circuit; and,

at least an EP-3DM level stacked on said substrate circuit, at least a portion of said EP-3DM level storing at least a portion of a form of test data for said CUT and being connected with said peripheral circuit through a plurality of inter-level connecting vias.

22. The IC supporting EP-3DMST according to claim 21, wherein said form of test data is a form of input test vectors (ITV).

23. The IC supporting EP-3DMST according to claim 22, wherein said form of ITV is ITV.

24. The IC supporting EP-3DMST according to claim 22, wherein said form of ITV is a source of said ITV.

25. The IC supporting EP-3DMST according to claim 24, wherein said source of said ITV is ITV seeds.

26. The IC supporting EP-3DMST according to claim 21, wherein said form of test data is a form of expected test vectors (ETV).

27. The IC supporting EP-3DMST according to claim 26, wherein said form of ETV is ETV.

28. The IC supporting EP-3DMST according to claim 26, wherein said form of ETV is a compressed ETV.

29. The IC supporting EP-3DMST according to claim 21, wherein said substrate circuit further comprises a plurality of test-vector buffers, said test-vector buffers storing at least a portion of said form of test data.

30. The IC supporting EP-3DMST according to claim 21, wherein said form of test data is downloaded into said CUT in a serial fashion.

31. The IC supporting EP-3DMST according to claim 21, wherein said form of test data is downloaded into said CUT in a parallel fashion.

32. The IC supporting EP-3DMST according to claim 21, wherein:

said CUT comprises a first CUT block and a second CUT block;

said substrate circuit further comprises a first test-vector buffer and a second test-vector buffer, said first test-vector buffer storing at least a portion of a form of test data for said first CUT block, said second test-vector buffer storing at least a portion of a form of test data for said second CUT block.

33. The IC supporting EP-3DMST according to claim 21, wherein said substrate circuit further comprises a D/A converter, said D/A converter converting at least a portion of said form of test data from digital into analog signals.

34. The IC supporting EP-3DMST according to claim 33, wherein said substrate circuit further comprises an analog comparator.

35. The IC supporting EP-3DMST according to claim 25, wherein said substrate circuit further comprises a data de-compressor for said ITV seeds.

36. The IC supporting EP-3DMST according to claim 26, wherein said substrate circuit further comprises a data comparator, said data comparator comparing said form of ETV for said CUT with a form of output test vectors (OTV) from said CUT.

37. The IC supporting EP-3DMST according to claim 28, wherein said substrate circuit further comprises a data compressor, said data compressor compressing OTV from said CUT.

38. The IC supporting EP-3DMST according to claim 21, wherein said substrate circuit further comprises a storage block, said storage block storing address information associated with mismatched OTV and ETV.

39. The IC supporting EP-3DMST according to claim 21, wherein said substrate circuit further comprises a multiplexor, the output of said multiplexor being selected from an external scan-test input, or from said EP-3DM.

40. The IC supporting EP-3DMST according to claim 21, wherein said substrate circuit further comprises a plurality of parallel-serial test flip-flops (PS-TFF), the output of said PS-TFF being selected from a normal data input, or from an external scan-test input, or from said EP-3DM.